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Document Title **Calorimeter Readout Control ASIC – GCRC V5 Design Description**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

Conceptual Design of the Glast Calorimeter Readout Control (GCRC) ASIC

(Ver 15)

Submission 5

DOCUMENT APPROVAL

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
Ver 5	9/24/01	Added command from TEM for calibration and described calibration function.
Ver 6	9/24/01	Added command from TEM for reading and writing of the GCRC configuration register.
Ver 7	10/03/01	Modified TEM address of GCRC configuration register and calibration command. Added description of GCRC hard wired addressing.
Ver 8	10/23/01	Defined Log Accept Bits Sent to TEM for each range of four-range readout. Modified diagrams to show GCRC not need data from TEM for read commands. GCRC now sends identical read data to TEM on both data lines.
Ver 9	11/08/01	Modified Command Function Bit Definitions. Added definition that TEM to GCRC command will preempt previous command if it has not completed. Modified GCFE Control waveforms to actual functionality of GCFE. Added specification that GCRC will have timer for GCFE responses, setting error bit in Status Register if times out with no response. Redefined that GCRC will transmit log-accept bits only in first range of 4-range readout. Removed ADC External Clock mode from configuration register. Added redundant Parity bit to configuration register.
Ver 10	11/28/01	Submission 1. Modify GCFE write diagram to show two extra DAQ_CLKs at the end. Add Write Key data pattern match for changing parity in configuration register. Change output signal names: ADC_CS\ to ADC_NCS, DAC_CS\ to DAC_NCS, RESETP to GRESETP, RESETM to GRESETM, STARTP to START_ACQP, STARTM to START_ACQM, CALIBP to CALIB_STRBP, CALIBM to CALIB_STRBM, RT_FIRST TO RIGHT_FIRST. Update Command Function Bit Definitions, table 3, to show new addressing for GCFE Ver 5 and above. GCRC maintains same function addressing. Added definition to CALIB_STRB signal that there will be a delay prior to signal assertion to GCFE chips.
Ver 11	1/22/02	Submission 2. Modify Chip pin assignments to move DAC_DATA_IN away from differential lines. Move Right_First to where DAC_DATA_IN was, move ADDR0 and ADDR1 up 1 pin number, put DAC_DATA_IN where ADDR0 was. Add extra redundant bit to GCRC Configuration Register for parity determination. Added Command Error bit to GCRC Status Register.
Ver 12	2/22/02	Submission 3. Not fabbed by Mosis.
Ver 13	4/23/02	Submission 4. Remove 3.2 usec delay between GCRC receiving Calib command from TEM and asserting Calib Strobe to front-end GCFE chips. Improved documentation for particular ADC used, added documentation for DAC write and reads. Added LVDS Drive and LVDS Receive Bias adjustment pins to the package drawing and pin definition list.
Ver 14	4/24/02	Submission 4. Removed wording of a dead time register from TEM command list, dead time register is non-existant.
Ver 15	2/7/03	Submission 5. Changed Read/Write address bit to 2 bit addressing. Function codes remain the same. Added TEM reset command functionality. Data readback from GCFE changed to half the system clock rate. Removed stretching and inhibiting of trigger requests to TEM. Added hard-wired GCRC version, readable at upper 8 MSBs of GCRC configuration register. Changed definition of Last Command error register to have leading MSB bit indicate whether error register bits start at TEM trigger command (MSB='0') or TEM command address bits (MSB='1'). Changed minimum spacing between range readout data to TEM from 25 to 31 clock cycles, Figure 17.

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1 PURPOSE

This document describes the conceptual design for the GLAST Large Area Telescope (LAT) Calorimeter Readout control (GCRC) ASIC.

2 SCOPE

This document gives an overrview over the conecptual architecture of the GLAST LAT Calorimeter Readout Control (GCRC) ASIC.

3 DEFINITIONS

3.1 Acronyms

GLAST – Gamma-ray Large Area Space Telescope

GCFE – Glast Calorimeter Front-end Electronics

GCRC – Glast Calorimeter Readout Control electronics

LAT – Large Area Telescope

TBR – To Be Resolved

CAL – Calorimeter Detector

TREQ – Level 1 Trigger Request

TEM – Tower Electronics Module

3.2 Definitions

Us, usec – Microsecond, 10^{-6} second

Dead Time – Time during which the instrument does not sense and/or record gamma ray events during normal operations..

s, sec – seconds

4 APPLICABLE DOCUMENTS

Documents that are relevant to the development of the GCFE concept and its requirements include the following:

4.1 Requirement Documents

GLAST00010, “GLAST Science Requirements Document”, P.Michelson and N.Gehrels, eds., July 9, 1999.

LAT-SP-00010, “GLAST LAT Performance Specification”, August 2000

LAT-SS-00018, “LAT CAL Subsystem Specification”, January 2001

4.2 Conceptual Design Documents

[1] GLAST Calorimeter Analog Front-End ASIC Design Consideration, Neil Johnson, NRL

[2] Conceptual Design of the GLAST Calorimeter Front End ASIC, Gunther Haller

[3] LAT Electronics System – Conceptual Design

[4] LAT Calorimeter Electronics System

[5] LAT GCFE Specification

[6] LAT TKR-CAL Tower Electronics Module – Conceptual Design

[7] LAT Control Protocol within LAT – Conceptual Design

[8] LAT Data Protocol within LAT – Conceptual Design

[9] LAT Housekeeping within LAT – Conceptual Design

[10] LAT L1 Trigger System – Conceptual Design

5 INTRODUCTION

The *GLAST* electronics system is described in [3]. The calorimeter sub-system electronics is documented in [4]. One of the two custom ASICs required is the Glast Calorimeter Readout Control (GCRC) Application Specific Integrated Circuit (ASIC). The basic function of the GCRC is the interface between the Tower Electronics Module (TEM) and the Glast Calorimeter Front End (GCFE) ASIC. The GCRC passes commands from the TEM to GCFEs, controls event readout of the log ends, and passes data back to the TEM. The GCRC is a digital chip with Low Voltage Differential Signalling (LVDS) Inputs and Outputs (I/O). Target fabrication processes for the ASIC are the 0.5 um Agilent CMOS and the 0.5 um Peregrine SOI.

The GCRC described in this document serves one calorimeter layer of one calorimeter side. There are four layers per calorimeter side, and four sides to the calorimeter.

The conceptual design in this document is based on interfaces required between the GCFE design documented in [3] and the TEM design documented in [6].

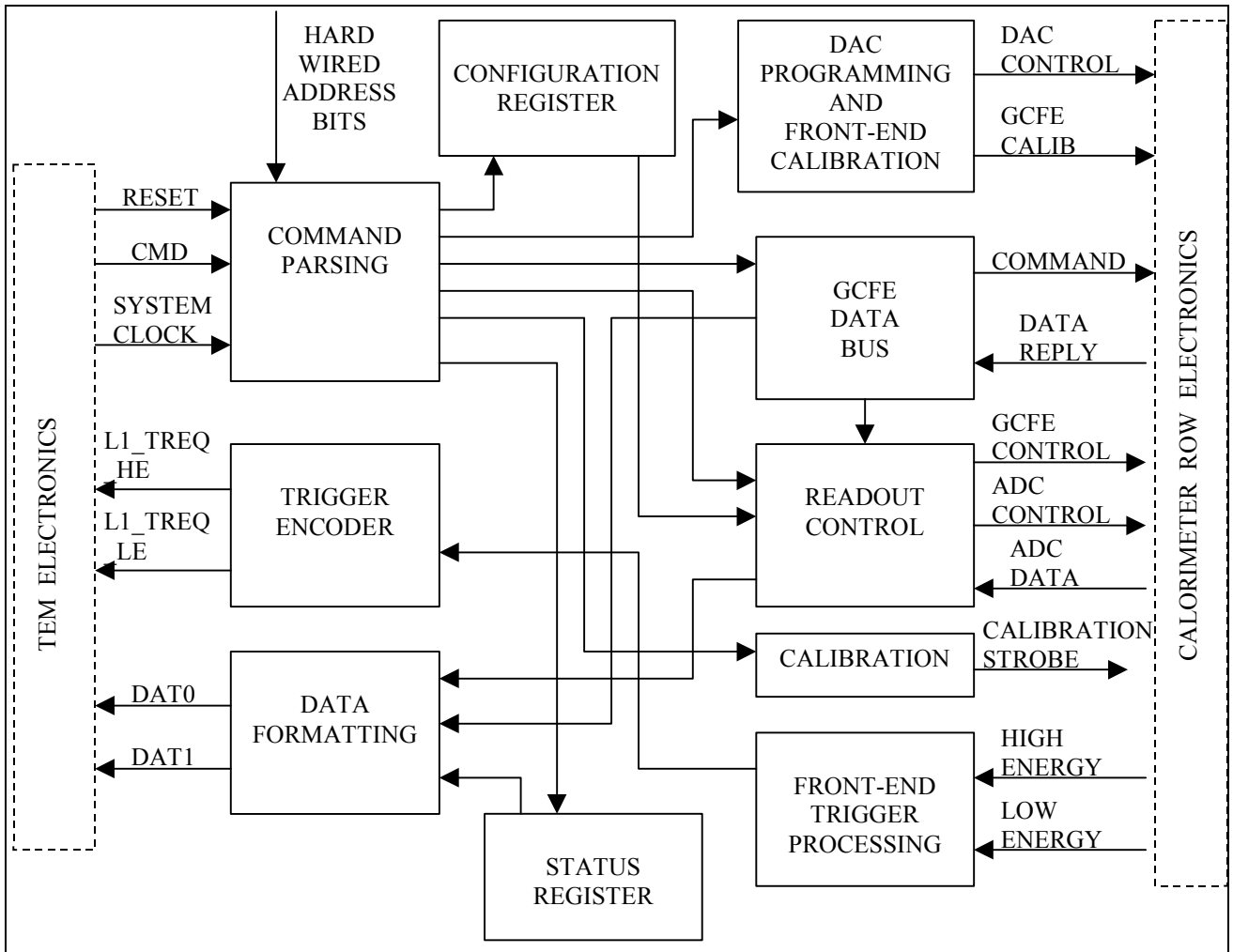

Figure 1. GCRC Block Diagram

6 GCRC Description

6.1 GCRC Overview

The GCRC ASICs are the interface between the 192 log-end GCFE ASICS and the single TEM, per tower module. The functionality of the GCRC is partioned such that one GCRC AISC interfaces one layer, 12 log ends, of the calorimeter. This calorimeter row partitioning follows from using "wired-OR" triggering per calorimeter row and calorimeter printed circuit board constraints of more horizontal routing space than vertical. The GCRCs receive a constant 20 MHz system clock from the TEM, the same clocking frequency of all communication with the TEM.

6.2 Command Parsing

Figure 1 includes a block for parsing of commands from the TEM. The TEM to GCRC command lines are bussed in parallel to all four GCFC ASICS per side of the calorimeter, refer to Figure 2.

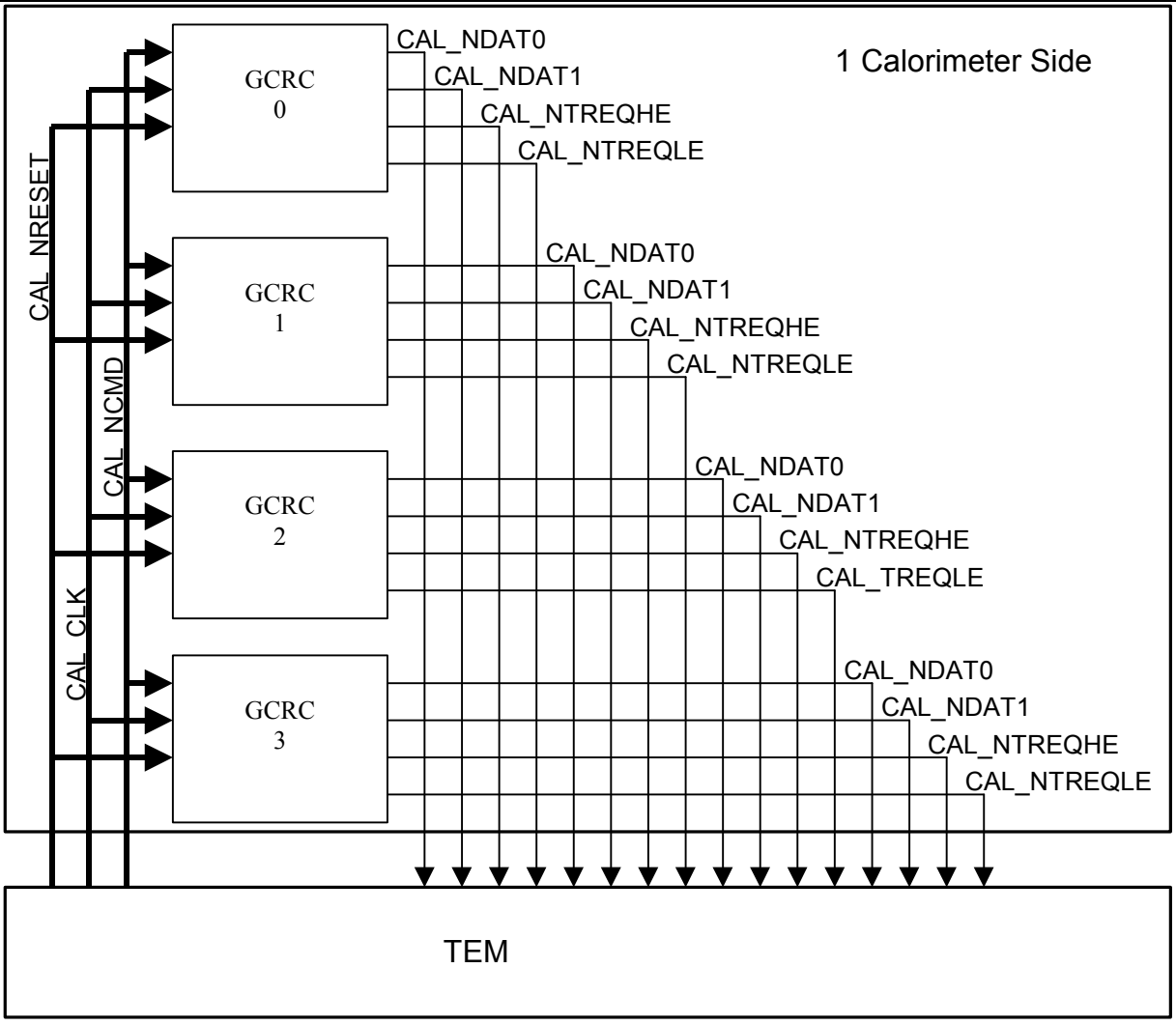

Figure 2. GCRC to TEM Communication Connection Diagram

Note that in comunication signal naming, signals between the TEM and GCRC begin with the letters "CAL_" indicating Calorimeter subsystem. Additionally, communication signals that are asserted low, have a "N" prefix in the root name. For example the signal name "CAL_NCMD" indicates it is a Command line (CMD) between the Calorimeter and TEM, asserted low. The asserted low differential signals are a good design practice because the fail-safe state is logic high. Differential signals in the figures are shown just prior to the differential driver or just after the differential receiver. Bit values in the document tables are shown in normal assertion high sense.

The TEM Command is one of four types:

a) Command Signal Readout (Trigger)

b) Command Register Load

c) Command Register Read

d) Dataless Command

The first bit in the TEM_CMD line following the start bit indicates a Signal Readout (Trigger) command or Load/Read/Dataless operation. If this Readout bit is asserted, then the command is for a Signal Readout (Trigger), and

the next bit determines the Readout Type. A parity bit follows the Signal Readout Type bit which is parity for the Signal Readout bit and the Readout Type bit. If the Signal Readout + Readout Type parity bit is incorrect, a single range readout process will occur and an error bit will be in the Status Register (Table 8). See Figure 3 for the timing diagram and Table 1 for bit definitions.

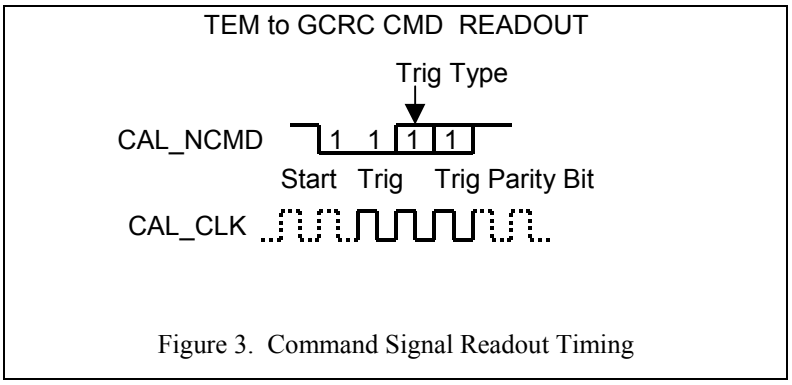

Figure 3. Command Signal Readout Timing

Table 1. Readout (Trigger) Type Bit Definitions

Bit Value	Definition
0 high	1 Readout Range
1 Asserted Low	4 Range Readout

The Read/Load/Dataless commands are either directed to a particular GCRC (row), particular GCFE (log end), or broadcast to all devices 'listening'. Register operations are initiated from the TEM by a not-asserted Signal Readout bit following the start bit. If the Signal Readout bit is not asserted and the trigger parity is incorrect, a single range readout is performed and an error is indicated in the status register (Table 8). An address follows the Signal Readout bits which generally points to a specifiec GCRC and GCFE device A GCFE Command Bit bit is included in the

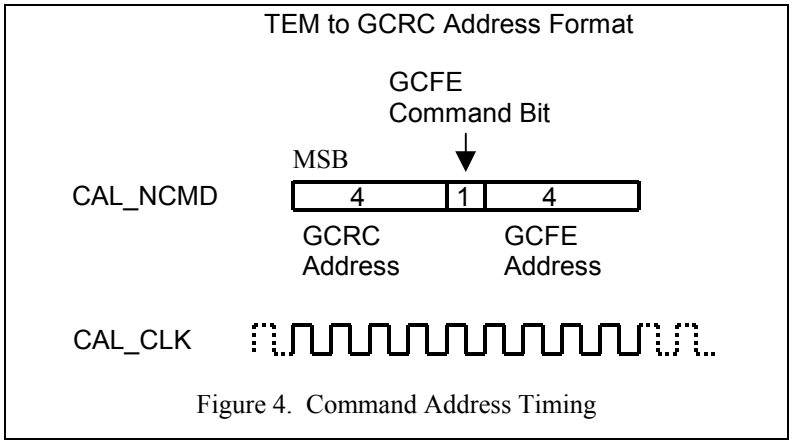

Figure 4. Command Address Timing

address to indicate whether the command is directed to a GCFE device, bit asserted, or GCRC device, bit unasserted. See Figure 4.

To facilitate device addressing, each of the four GCRCs per calorimeter side and each of the 12 GCFE's per row has a unique hard-wired address for decoding the command address bits.

Table 2. GCRC Hard-Wired Addressing

Addr3	Addr2	Addr1	Addr0	GCRC Resonds to Command Address
0	0	0	0	0000 and 1111
0	0	0	1	0001 and 1111
0	0	1	0	0010 and 1111
0	1	1	1	0111 and 1111

Upon a GCRC chip decoding a command with GCRC address matching its wired address (See Table 2), and the Address/Function parity checks good, the GCRC has two options:

a) GCFE Command Bit not asserted: Decode function bits at the GCRC and act upon command See Figure 5 and Figure 6

b) GCFE Command Bit asserted: forward command to GCFE's on row stripped of GCRC address and parity bits. See Figure 7 and Figure 8.

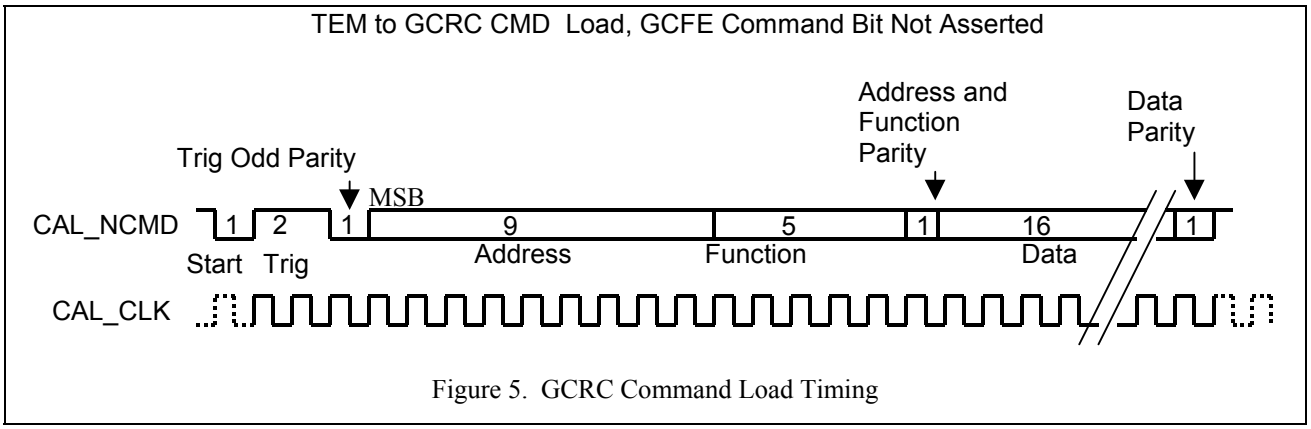

Figure 5. GCRC Command Load Timing

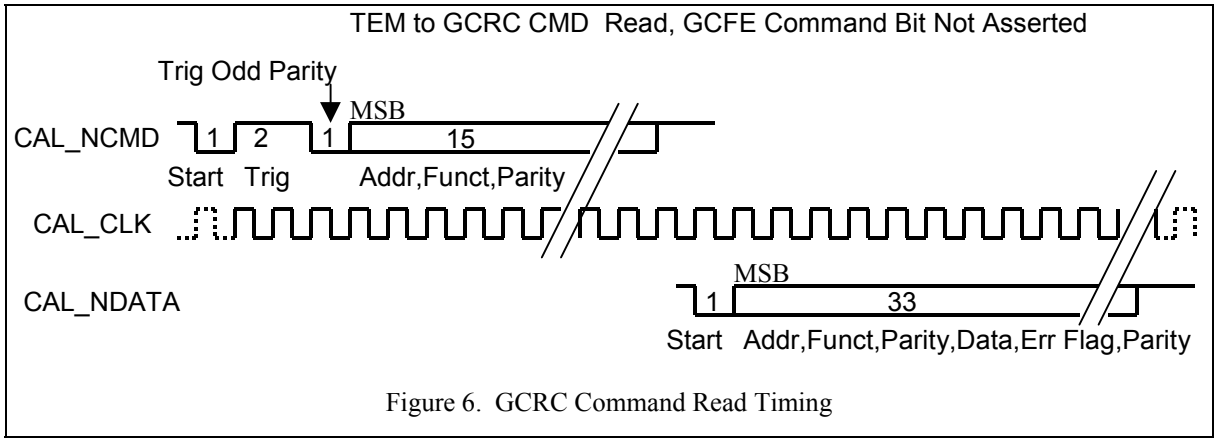

Figure 6. GCRC Command Read Timing

Figure 5 shows the command structure to load a GCRC register. Figure 6 shows the structure for GCRC register read. Note that the GCRC does not use data from the TEM for a read command. The returned address and function bits are repeated from the command. The parity bits are recomputed, according to the parity type set in the GCRC configuration register, Table 7. The returned data parity is computed on the returned data and Error Flag bit. The

GCRC returns identical command data on both CAL_NDATA0 and CAL_NDATA1, thus the un-numbered NDATA is used in the diagram.

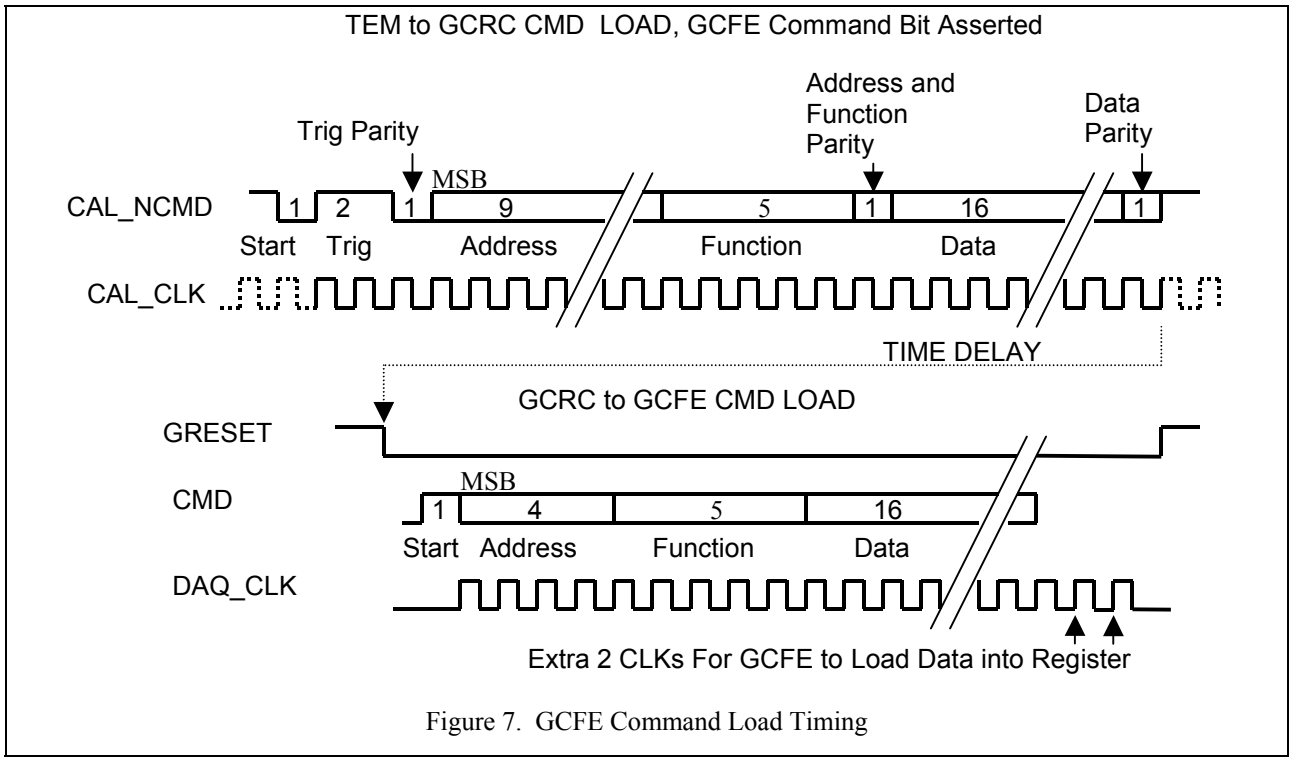

Figure 7. GCFE Command Load Timing

Figure 7 shows the command structure for a GCFE Load command. Note that the GCRC forwards the command stripped of the GCRC address and parity bits. Also, the command is only forwarded after all parity bits check correctly.

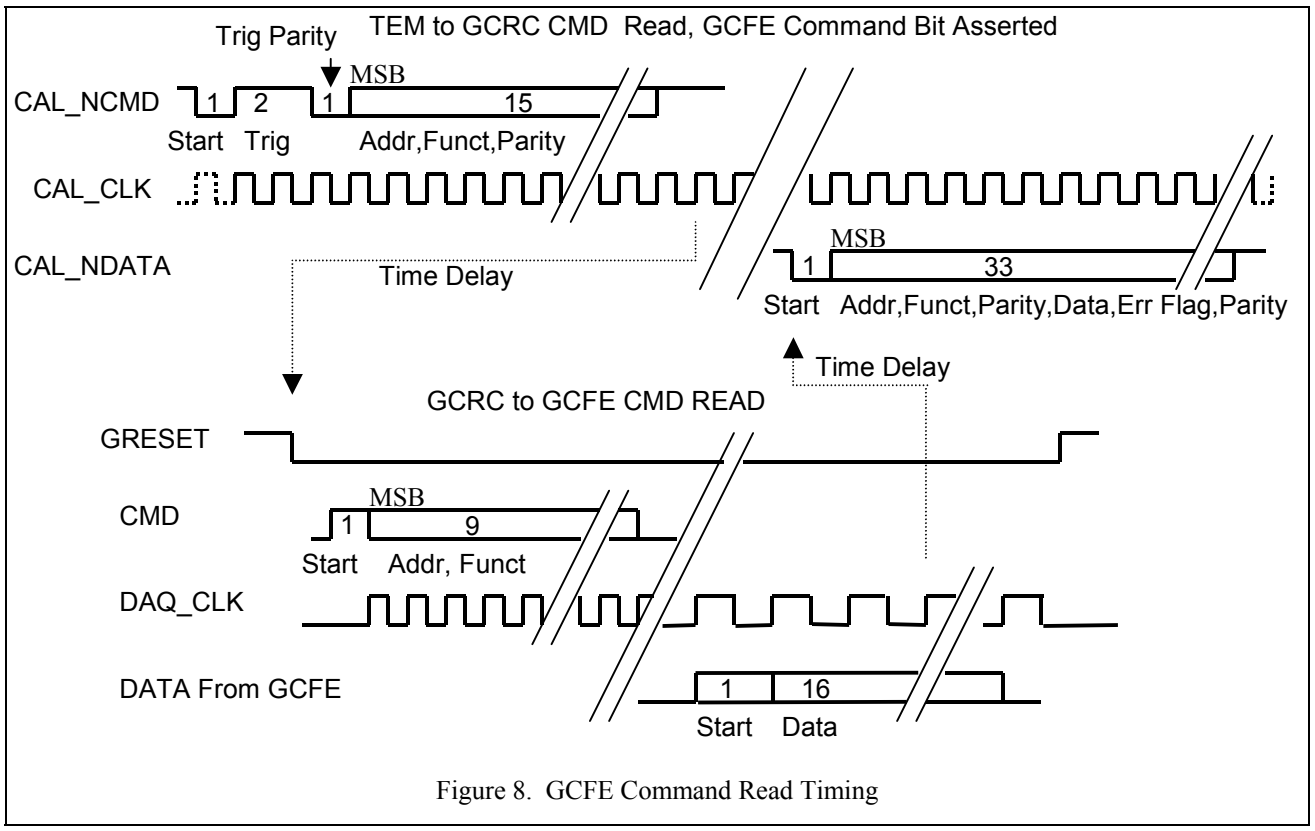

Figure 8. GCFE Command Read Timing

Figure 8 shows the command structure for GCFE Read command. Note again that the GCRC forwards the command stripped of the GCRC address and parity bits. Since no data is sent to the GCFE with a read command, the command can be sent to the GCFE following the Address/Function parity bit checking correctly. The reply to the TEM is rebuilt using the original address and function bits from the command, with parity recomputed according to the GCRC configuration register. The returned data is that data returned from the GCFE chip addressed in the command. Returned data is clocked out of the GCFE chip at half the Cal_Clk rate. The data parity is computed on the returned data and Error Flag bit, parity format according to the GCRC configuration register (Table 7). The GCRC begins transmitting back to the TEM upon receipt of the second data bit from the addressed GCFE.

If there are any errors in the described processes, 16 bits of the received command is saved in a error register and a global GCRC error flag is set. The error flag status is sent back to the TEM at the end of the next read command. The error flag is reset following transmission of its status. The command error register is readable by command (see Table 5).

The GCRC will timeout if an expected response from a GCFE does not occur. The GCRC will set an error bit in the GCRC status register, Table 8, and send a reply to the TEM with a zero data field and error bit set true.

The TEM performs data flow control between the TEM and GCRC. The GCRC will always act upon the most current received command, preempting the previous command if it has not been completed.

Communication with the TEM on the CAL_NCMD line and the CAL_NDAT0 line is performed with Low Voltage Differential Signalling (LVDS) asserted low.

6.3 GCFE Data Bus

The GCRC log-end commands are bussed in parallel to the GCFE chips. The 12 GCFE chips per GCRC have four uniquely hard-wired address lines to decode the addressed command. The commands to the GCFE chips use LVDS lines. The GCRC receives reply data back through individual LVDS data lines from each GCFE chip.

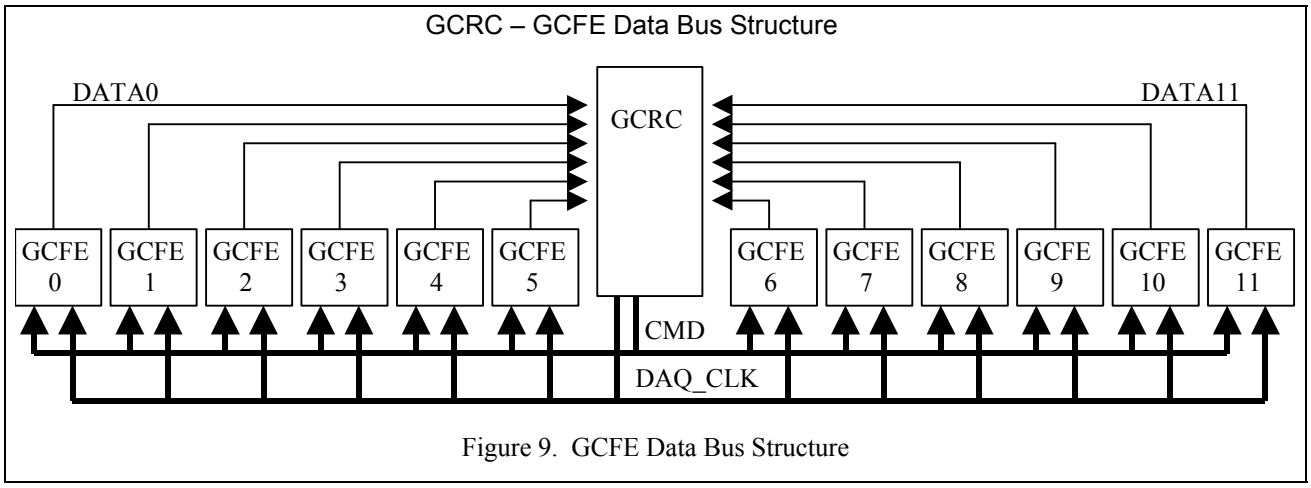

Figure 9. GCFE Data Bus Structure

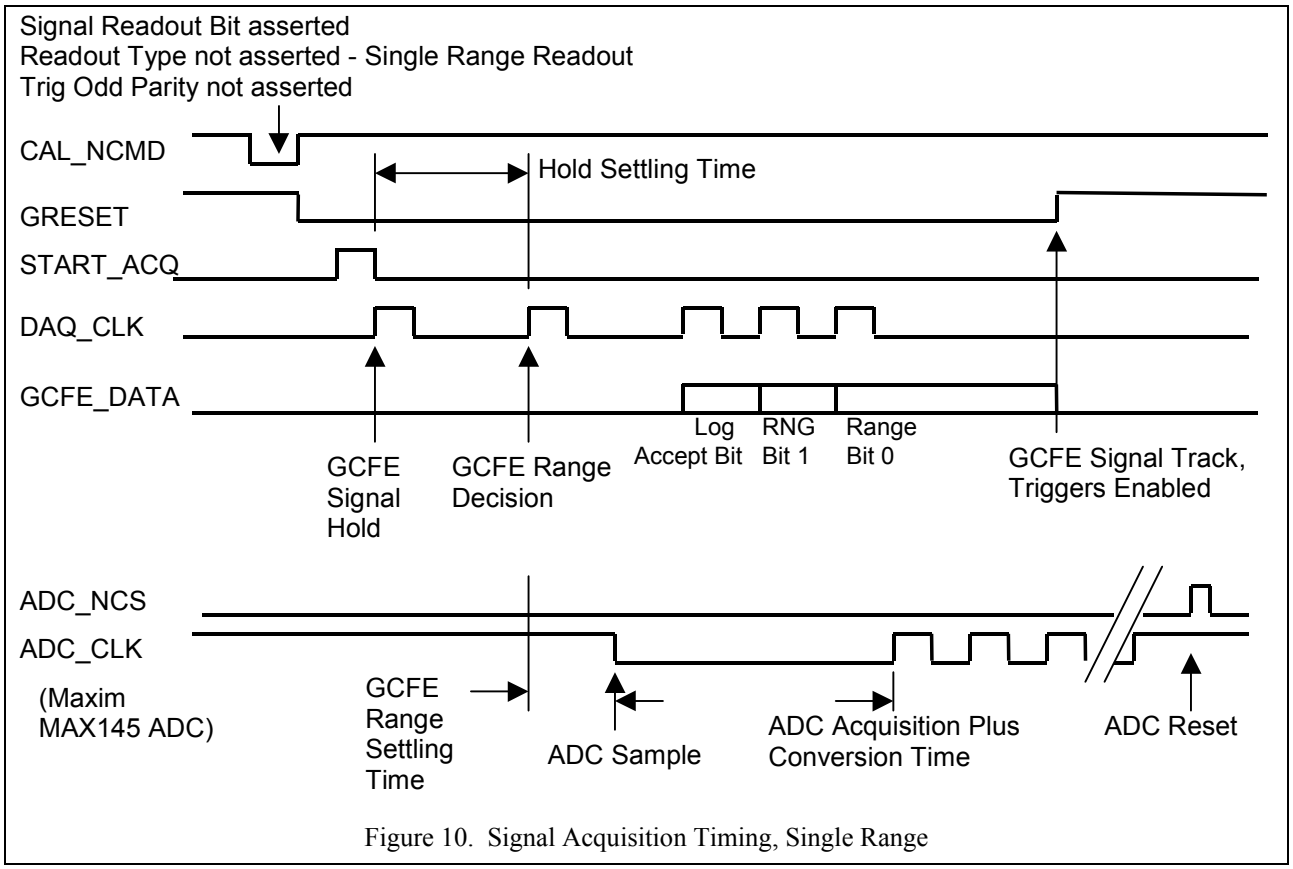

Figure 10. Signal Acquisition Timing, Single Range

6.4 Readout Control

Upon receiving a Signal Readout (trigger) command, the GCRC immediately executes a readout cycle by directing the GCFE chips through the signal acquisition cycle, and controlling the digitization by the ADCs. Refer to Figure 10.

The nominal readout is digitization of one of the four possible GCFE ranges. Additionally, the GCRC can be directed, through the CAL_NCMD line to digitize all four GCFE ranges, as shown in Figure 11

Through prior TEM commanding, each GCFE chip is nominally allowed to decide its own optimum range to readout per event. Thus for correct association of the ADC data, the GCRC readout control reads two range defination data bits from each GCFE chip, per range digitized. The range defination bits are passed with the ADC data to the TEM.

Zero supression, the process of discarding minimal amplitude data, is made easier with a dedicated discriminator bit in each GCFE chip. The GCRC reads this bit, termed 'Log-Accept Bit' , from each GCFE chip during the first range readout cycle. This bit is again passed with the ADC data, enabling the TEM to quickly zero suppress data with no computation.

6.5 Data Formatting

Data sent to the TEM is of two varities:

a) Register data following a Read Register command

b) Log-end digitized data following a Signal Readout command.

There is no indicator in the bitstream for the two varities of data. But since both are returned from TEM commands, the TEM knows which type of data is returned.

There are two data lines, CAL_NDATA0 and CAL_NDATA1 for sending data to the TEM. Both CAL_NDATA0 and CAL_NDATA1 return identical command read data. For event readout, CAL_NDATA0 returns half the ADC data

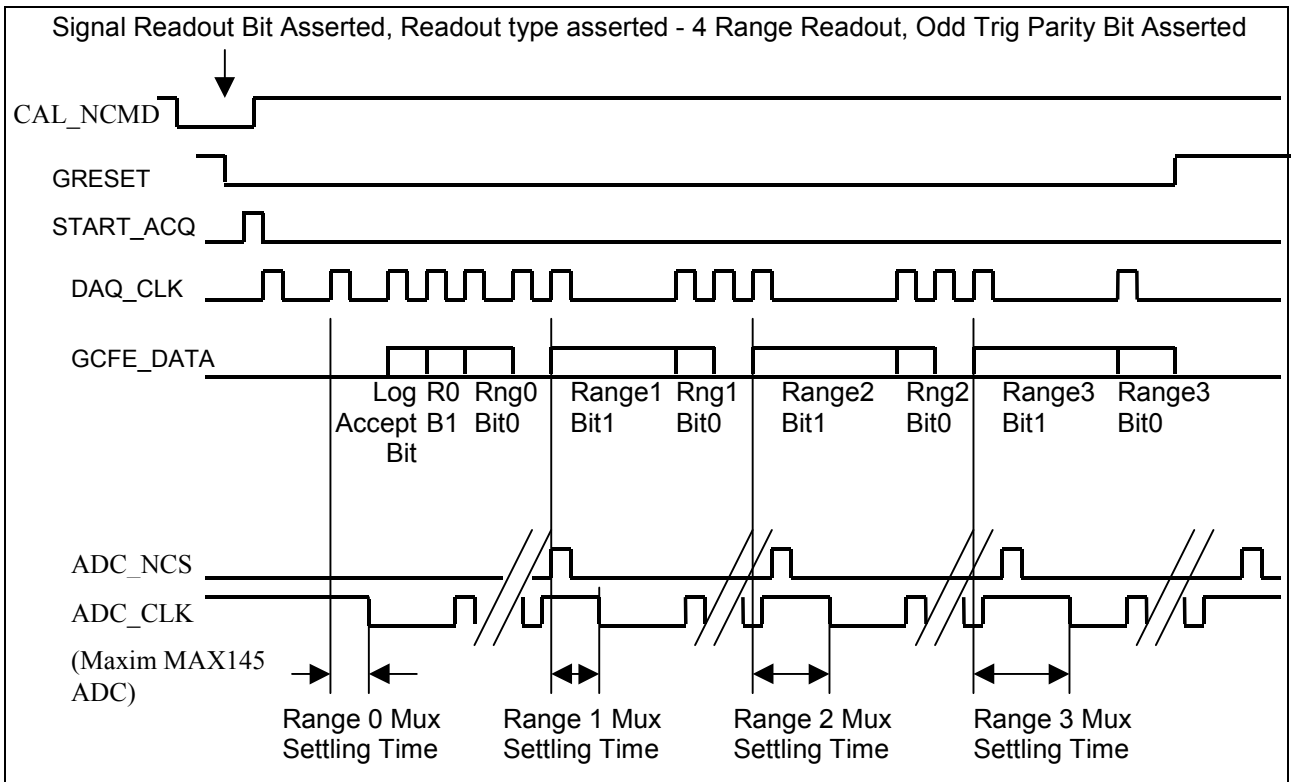

Figure 11. Signal Acquisition Timing, Four Range

and CAL_NDATA1 returns the other half of the data. The two data lines get the ADC data off the calorimeter board quicker to meet a calorimeter dead time goal of 20 usec.

For register data, the returned data format is shown in Figure 12.

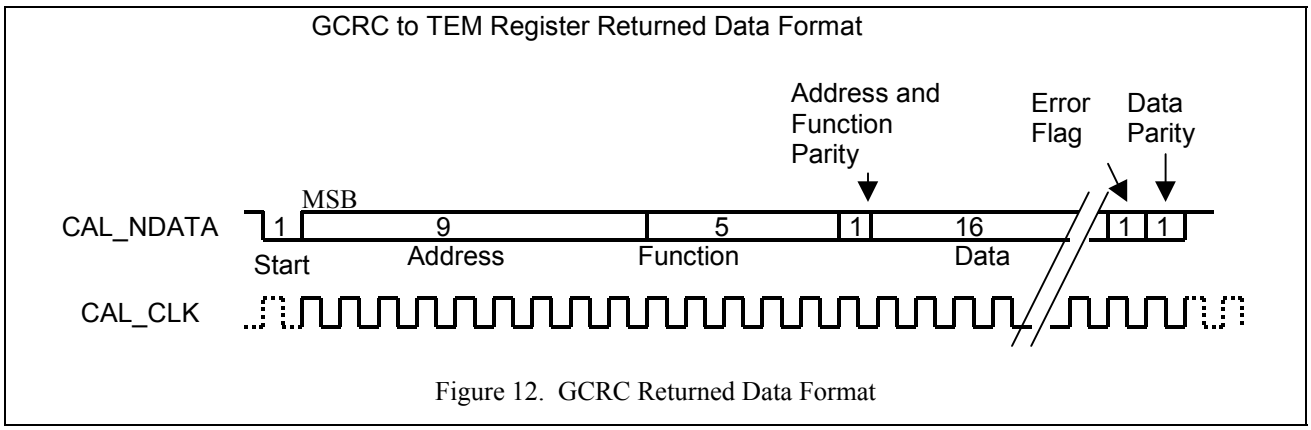

Figure 12. GCRC Returned Data Format

The Address and Function bits are repeated from the initiating command. The Address/Function parity bit is recomputed in accordance to the parity selected in the GCRC configuration register (Table 7). The data is returned is a copy from the register selected. The error flag is asserted if there has been any type of error in the GCRC commanding. The error flag register is cleared following transmission.

For Signal Readout the general data order is shown in Figure 13 and Figure 14. Figure 13 shows line CAL_DATA0 starting with Log-end/ADC 0 and incrementing, line CAL_DATA1 starting with Log-end/ADC 11 and decrementing. Figure 14 shows the dependancy of the data order with Right_First input pin level. If the Right_First input is asserted high, the data normally sent on Cal_NDATA0 is sent on Cal_NDATA1 and visa-versa. With this feature, data streams from opposite log-ends (opposite calorimeter circuit boards) can be alligned to arrive concurrently at the TEM.

Figure 15 and Figure 16 show the details for the interleaved (without associated grouping) Log-end/ADC bits in the readout The GCFE range bits and zero suppression (log-accept) bits are sent to the TEM ahead of the ADC data, with ordering similar to that of the ADC bits. The ADC bits are sent to the TEM interleaved to get the bits off the calorimeter more quickly

Figure 17 shows the transmission format for a four-range readout. The first range (Range 0) data is identical to the single range readout format. The following ranges (Ranges 1 to 3) transmit in similar format except for not transmitting the log accept bits. Thus readout ranges 1,2 and 3 transmit 6 fewer bits (85 bits) in each packet. For TEM processing, there is a spacing requiremnt of a minimum 25 system clock cycles between range transmissions.

The data lines are implemented with LVDS, asserted low levels.

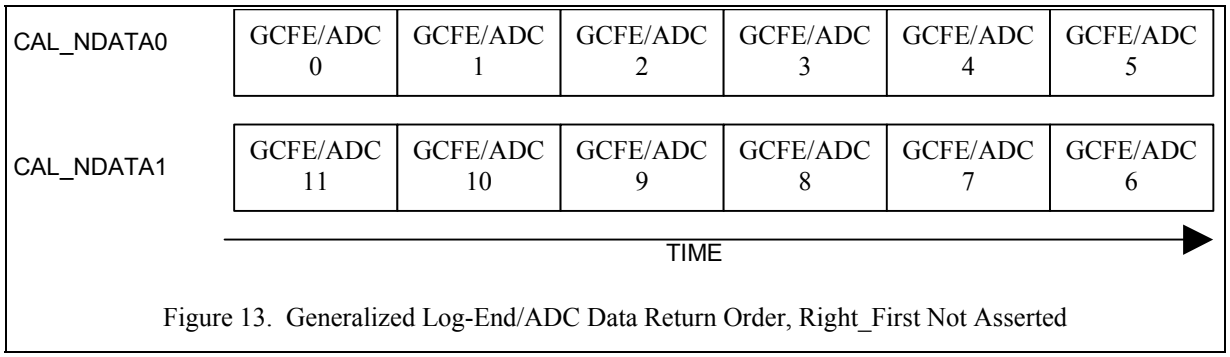

Figure 13. Generalized Log-End/ADC Data Return Order, Right_First Not Asserted

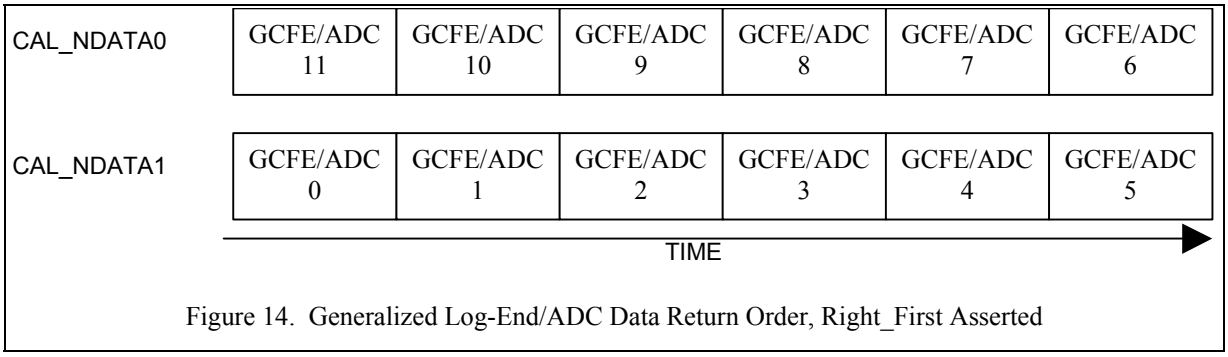

Figure 14. Generalized Log-End/ADC Data Return Order, Right_First Asserted

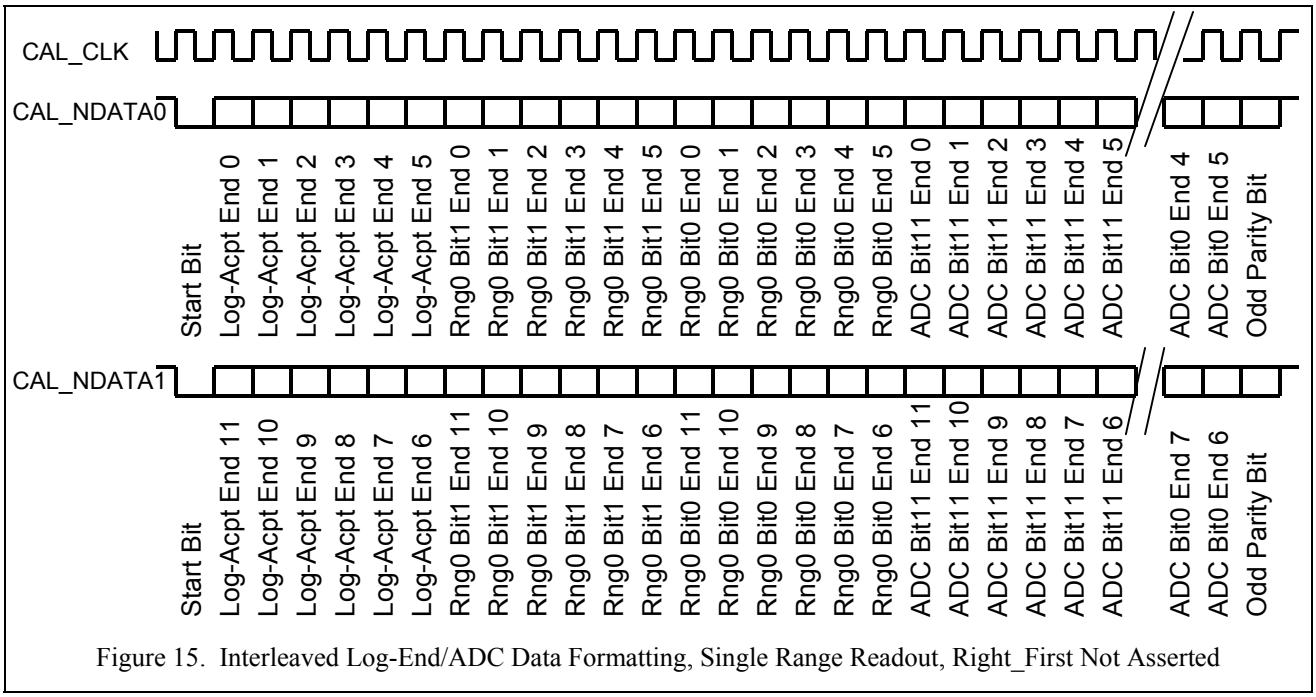

Figure 15. Interleaved Log-End/ADC Data Formatting, Single Range Readout, Right_First Not Asserted

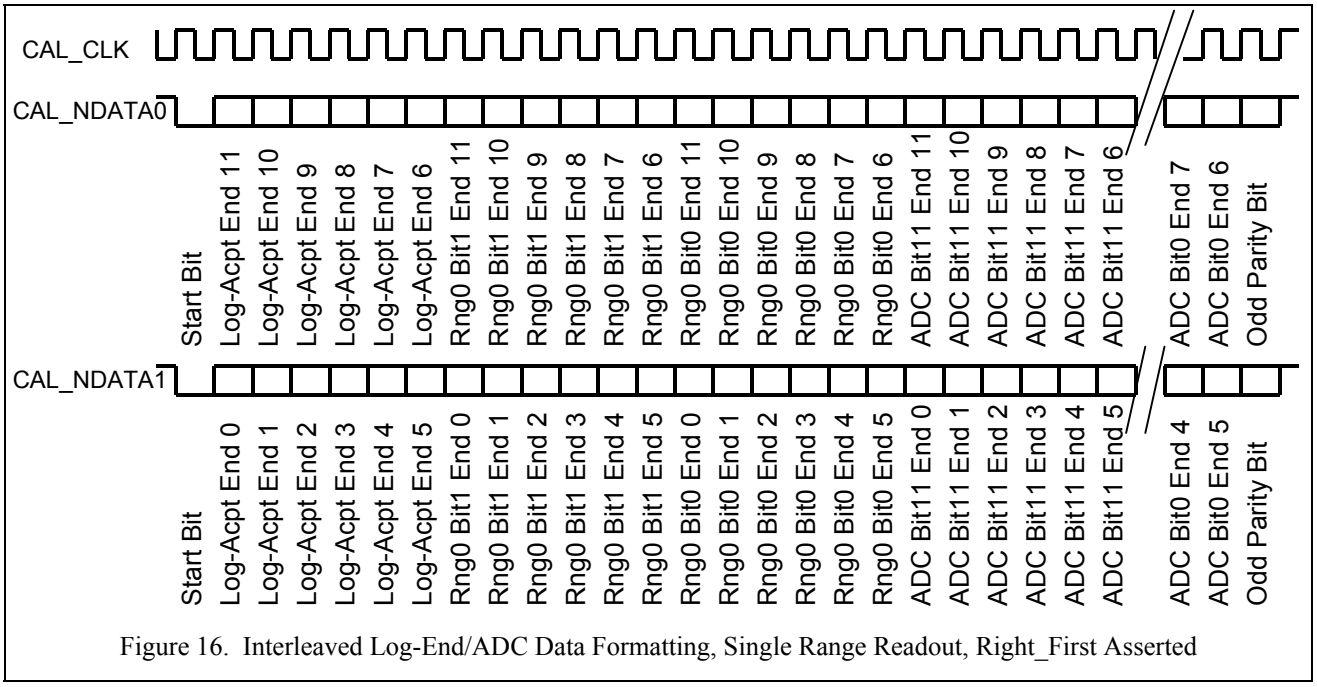

Figure 16. Interleaved Log-End/ADC Data Formatting, Single Range Readout, Right_First Asserted

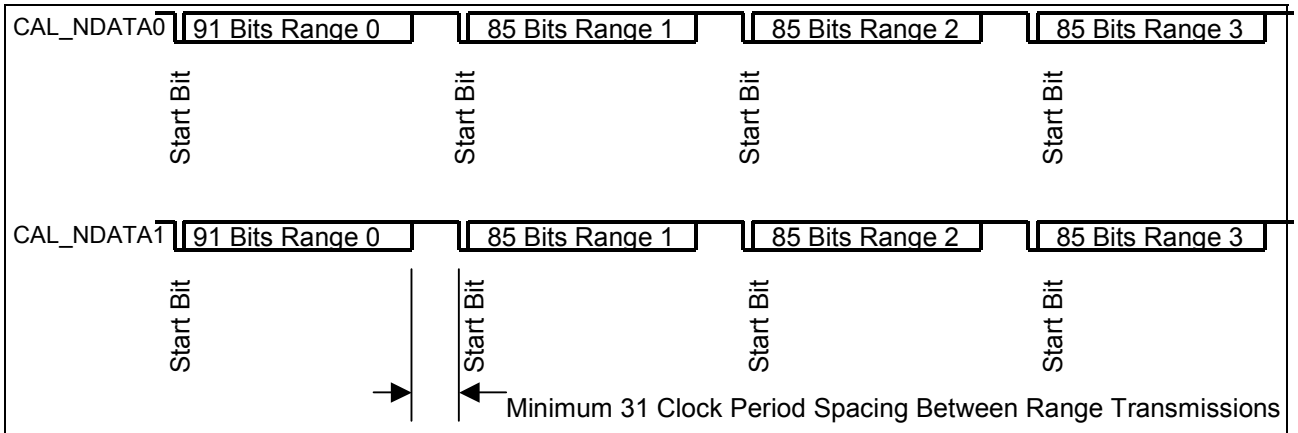

Figure 17. Log-End/ADC Data Formatting, Four Range Readout Note that ranges 2 to 4 do not send log-accept bits.

6.6 Calibration

The Calorimeter front-end electronics are in part calibrated with charge injection into the GCFE front-end preamplifiers. The CALIB_STRB signal from the GCRC is used to inject an amount of charge proportional to the external DAC voltage setting, into the row of GCFE preamplifiers.

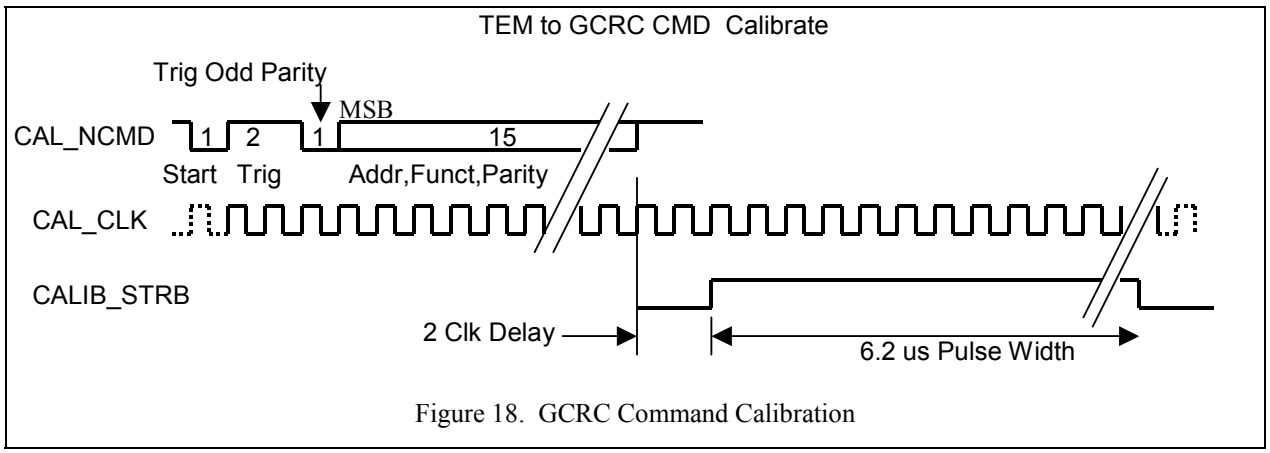

Figure 18. GCRC Command Calibration

Figure 18 shows that the GCRC asserts the CALIB_STRB signal to the row of GCFE chips immediately following reception of the Calibration command from the TEM (Table 5). The CALIB_STRB is a fixed pulse width of 6.2 microseconds, long enough that the analog signal is sampled prior to the falling edge of CALIB_STRB. The TEM may command a trigger request to the GCRC during the CALIB_STRB asserted high period, therefore the GCRC will be able to process further commands or trigger requests from the TEM during the Calibration pulse period.

The Calibration lines are implemented with LVDS, asserted positive.

6.7 Trigger Encoding

Trigger requests to the TEM are on the CAL_NTREQHE and CAL_NTREQLE lines. The signaling format is minimum pulse width of 50 nsec, and maximum pulse length is time-over-threshold. The trigger communication lines between the GCRC and TEM are LVDS, asserted low.

6.8 Front-End Trigger Processing

The High Energy and Low Energy Wired-OR triggers, HE_NDISC and LE_NDISC, from the GCFE chips are sampled on the rising system clock edge. They are twice sampled by flip-flops prior to forwarding to the TEM, resulting in a propagation delay to the TEM of two system clock periods.

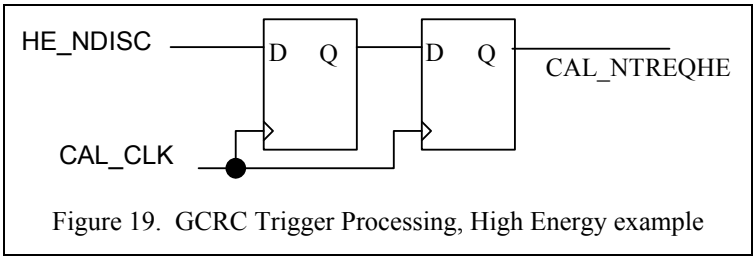

Figure 19. GCRC Trigger Processing, High Energy example

6.9 Reset

Resets of the GCRC are performed on the CAL_NRESET input line or by TEM command (Table 5) on the data line . The CAL_NRESET line is continually sampled at the system clock rate. The CAL_NRESET input is a differential LVDS input asserted low. When a Reset Command is determined eirther by the dedicated reset line or TEM Command, the GCRC holds itself in Chip Reset for 15 clock cycles. Figure 20 below shows that the dedicated line Reset is determined by sampling a high CAL_NRESET line followed by three successive low CAL_NRESET samples.

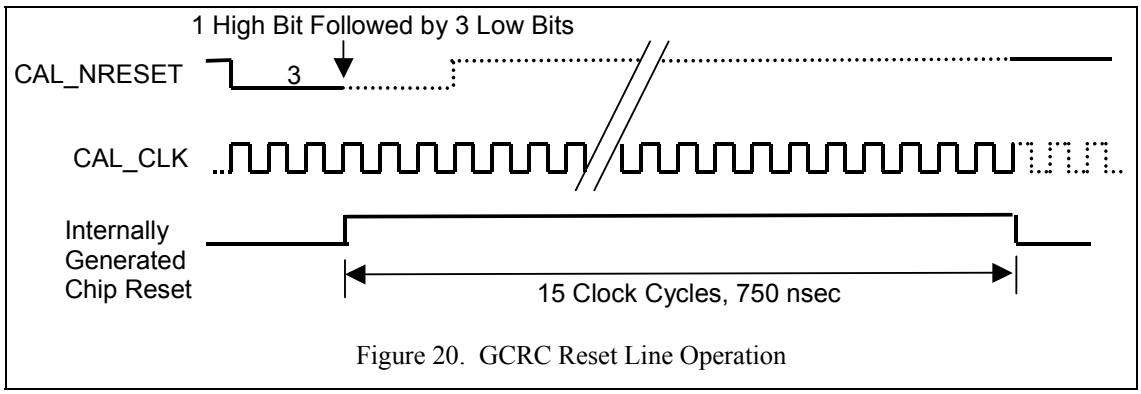

Figure 20. GCRC Reset Line Operation

Table 3. Register Reset Operation

Register	Reset Function		Register	Reset Function
Time Delay 1, Peak Hold to GCFE Range decision	Register unchanged		Digital to Analog Converter (DAC) setting	Zero register
Time Delay 2, GCFE Range decision to ADC sample	Register unchanged		GCRC configuration register	Zero 3 least significant bits. GCRC version bits fixed.
Time Delay 3, ADC Conversion time	Register unchanged		Status Register	Zero register
			Last Command Error Register	Zero register.

Table 3 above shows the effect of reset upon the GCRC registers. Registers constructed from Single Event Upset immune flip-flops are not clearable, and thus do not get changed.

6.10 On Board DAC Programming and Reading.

The GCRC can program an onboard Digital to Analog Converter (DAC), Maxim MAX5121, from a TEM command. The onboard DAC is used for calibration of the GCFE chips. The GCRC passes the 16 bit data field of the DAC Write command directly to the onboard DAC. 12 of the DAC data bits control the DAC output voltage, the remaining bits formulate the DAC operation, as described in Table 4. The onboard DAC is programmed by a 5 MHz serial data stream from the GCRC. As the GCRC is pushing data bits into the onboard DAC, the previous DAC-held data bits are being taken in by the GCRC. A TEM DAC Read command returns these previous DAC data bits, the bits pushed out by the last DAC write command . Thus a TEM DAC Read command returns the second-to-last DAC write command. Successive DAC read commands return the same value. The timing of the DAC read command is the same as any GCRC register, as shown in Figure 6. The timing of the DAC write operation is longer due to the reduced rate serial communication, and is shown in Figure 21. The GCRC will be able to handle any TEM command immediately following a DAC Write command except another DAC Write command.

Table 4. Onboard DAC, Maxim MAX5121, Program Bits

B15	B14	B13	B12-B1	B0	Description
0	0	0	Don't Care	0	No Operation
0	1	0	12 Bit DAC value	0	DAC Write

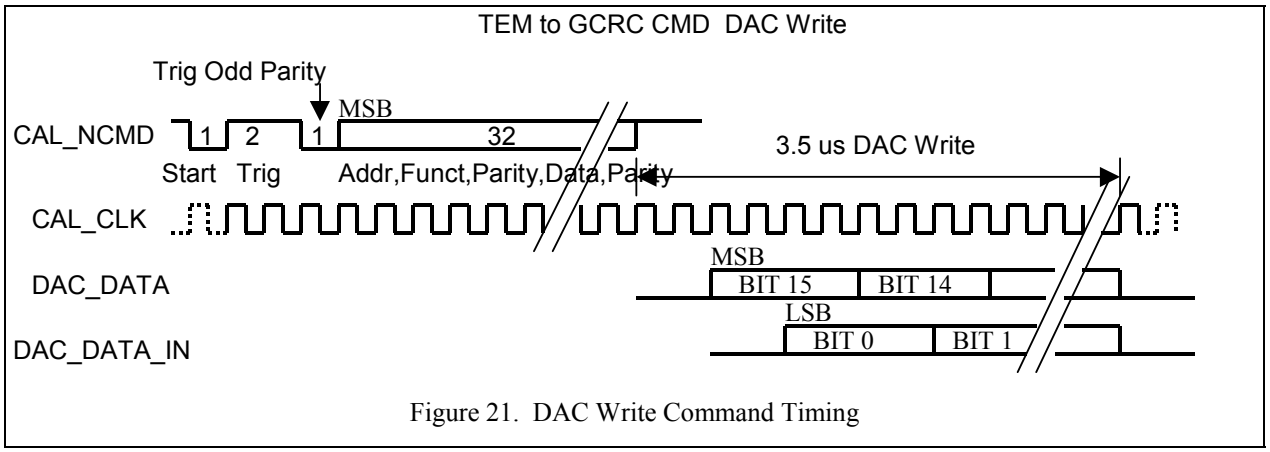

Figure 21. DAC Write Command Timing

6.11 Operational Parameter Registers

Table 5. Command Function Bit Definitions

GCRC Ver <=4 Function Bits	GCRC Ver >=5 Function Bits	Definition	Data Bits 15-8 Write Key	Number of Data Bits
00000	00000	Write not used		
Not Implemented	00001	Write Reset GCRC		0
00011	00011	Calibration strobe command		0
01000	*01000*	*Write GCFE Config Reg 0*		*13 bits*
10000	*10000*	*Read GCFE Config Reg 0*		
01001	*01001*	*Write GCFE Config Reg 1*		*7 bits*
10001	*10001*	*Read GCFE Config Reg 1*		
01010	*01010*	*Write GCFE Fast Low Energy DAC*		*7 bits*
10010	*10010*	*Read GCFE Fast Low Energy DAC*		
01011	*01011*	*Write GCFE Fast High Energy DAC*		*7 bits*
10011	*10011*	*Read GCFE Fast High Energy DAC*		
01100	*01100*	*Write GCFE Log Accept DAC*		*7 bits*
10100	*10100*	*Read GCFE Log Accept DAC*		
01101	*01101*	*Write GCFE Upper Level Discrim DAC*		*7 bits*
10101	*10101*	*Read GCFE Upper Level Discrim DAC*		
01110	*01110*	*Write GCFE Reference DAC*		*7 bits*
10110	*10110*	*Read GCFE Reference DAC*		
01011	01011	Write Time Delay 1, Peak Hold to GCFE Range decision		6 bits
11011	10011	Read Time Delay 1, Peak Hold to GCFE Range decision		6 bits
01100	01100	Write Time Delay 2, GCFE Range decision to ADC sample		6 bits
11100	10100	Read Time Delay 2, GCFE Range decision to ADC sample		6 bits
01101	01101	Write Time Delay 3, ADC Conversion time		8 bits
11101	10101	Read Time Delay 3, ADC Conversion time		8 bits
01110	01110	Write Digital to Analog Converter (DAC) setting		16 bits
11110	10110	Read Digital to Analog Converter (DAC) setting		16 bits
01111	01111	Write GCRC configuration register	A5	3 bits
11111	10111	Read GCRC configuration register. GCRC Version Number is 8 most significant bits.		3 bits
10000	10000	Read Status Register		5 bits
10001	10001	Read Last Command Error. Reference Table 6.		16 bits

Table 5 shows the address space reserved for the GCRC function bit mapping: For GCRC ver 4 and earlier, the first bit of the 5 bit function field indicates read - bit "1", or write - bit "0". For GCRC ver 5 and later, the first two bits of the 5 bit function field indicates read – bits "10", write "01", or dataless command "00". Table 5 shows pass-through commands to the GCFE in italics. Table 6 defines the bits in the Last Command Error register. Table 7 defines the GCRC configuration register and Table 8 defines the GCRC Status Register.

Table 6. Last Command Error Register Bit Configuration

Last Error Register MSB	**Bit 14 – Bit 0, LSB**
0	2 Trig Bits, 1 Trig Parity Bit, 9 Address Bits, 3 Function Bits
1	9 Address Bits, 5 Function Bits, 1 Address-Function Parity Bit.

Table 7. GCRC Configuration Register Bit Definition

Bit	**Definition**
0 LSB	GCRC Parity Bit A, Default value 0.
1	GCRC Parity Bit B, Default value 0.
2	GCRC Parity Bit C, Default value 0. Default Parity is Odd, at least one of Parity Bit A, B, C is value 0. Even Parity is all of Parity Bits A, B and C set to 1.

Table 8. GCRC Status Register Bit Definition

Bit	**Definition**
0 LSB	TEM Trigger Parity Error occurred
1	TEM Commmand Address and Function Parity Error occurred
2	TEM Data Parity error occurred
3	GCFE Read Timeout
4	TEM Command Error. Commanded address and parity corrrect, but not recognized read, write or dataless function command.

7 Pin Names

Table 9. Input Pin Definitions

DATA0P to DATA11P	Data from GCFE chips, Positive LVDS, asserted high
DATA0M to DATA11M	Data from GCFE chips, Negative LVDS, asserted low
HE_NDISCP	GCFE "Wired-OR" High Energy layer trigger, Pos LVDS, asserted low
HE_NDISCM	GCFE "Wired-OR" High Energy layer trigger, Neg LVDS, asserted high
LE_NDISCP	GCFE "Wired-OR" Low Energy layer trigger, Pos LVDS, asserted low
LE_NDISCN	GCFE "Wired-OR" Low Energy layer trigger, Neg LVDS, asserted high
ADC0_DAT to ADC11_DAT	ADC Data from each Log End
ADDR0 to ADDR3	Hard-Wired GCRC Address, Bits 0,1,2,3
CAL_RIGHT_FIRST	Control Bit, Swaps log-end left/right readout order when asserted high
DAC_DATA_IN	Input Data Readback from DAC
CAL_NCMDP	Command from TEM, Positive LVDS, asserted low
CAL_NCMDM	Command from TEM, Negative LVDS, asserted high
CAL_CLKP	System Clock from TEM, Positive LVDS, asserted high
CAL_CLKM	System Clock from TEM, Negative LVDS, asserted low
CAL_NRESETP	Reset from TEM, Positive LVDS, asserted low
CAL_NRESETM	Reset from TEM, Negative LVDS, asserted high
LVDS_DRV_BIAS	Bias Adjustment. Resistor to Gnd increases drive current, minimizes time delay.
LVDS_RECV_BIAS	Bias Adjustment. Resistor to Vdd increases receiver current, minimizes time delay.

Table 10. Output Pin Definitions

DAQ_CLKP	Clock to GCFE chips, Positive LVDS, asserted high
DAQ_CLKM	Clock to GCFE chips, Negative LVDS, asserted low
CMDP	Command to GCFE chips, Positive LVDS, asserted high
CMDM	Command to GCFE chips, Negative LVDS, asserted low
GRESETP	Reset to GCFE chips, Positive LVDS, asserted high
GRESETM	Reset to GCFE chips, Negative LVDS, asserted low
START_ACQP	GCFE Start Acquisition Cycle, Positive LVDS, asserted high
START_ACQM	GCFE Start Acquisition Cycle, Negative LVDS, asserted low
CALIB_STRBP	Calibration Strobe to GCFE chips, Positive LVDS, asserted high.
CALIB_STRBM	Calibration Strobe to GCFE chips, Positive LVDS, asserted low.
ADC_NCS	ADC Chip Select, asserted low
ADC_CLK	ADC Clock
DAC_NCS	Calibration DAC Chip Select, asserted low
DAC_CLK	Calibration DAC Clock
DAC_DATA	Calibration DAC Data
CAL_NTREQHEP	L1 Trigger Request to TEM, High Energy, Positive LVDS, asserted low
CAL_NTREQHEM	L1 Trigger Request to TEM, High Energy, Negative LVDS, asserted high
CAL_NTREQLEP	L1 Trigger Request to TEM, Low Energy, Positive LVDS, asserted low
CAL_NTREQLEM	L1 Trigger Request to TEM, Low Energy, Negative LVDS, asserted high
CAL_NDATA0P	Data to TEM, “Pipe” 0, Positive LVDS, asserted low
CAL_NDATA0M	Data to TEM, “Pipe” 0, Negative LVDS, asserted high
CAL_NDATA1P	Data to TEM, “Pipe” 1, Positive LVDS, asserted low
CAL_NDATA1M	Data to TEM, “Pipe” 1, Negative LVDS, asserted high

Table 11. Power Pin Definitions

VCC	Digital Supply, noninally 3.3 Volts
GND	Digital ground

Pin Numbers

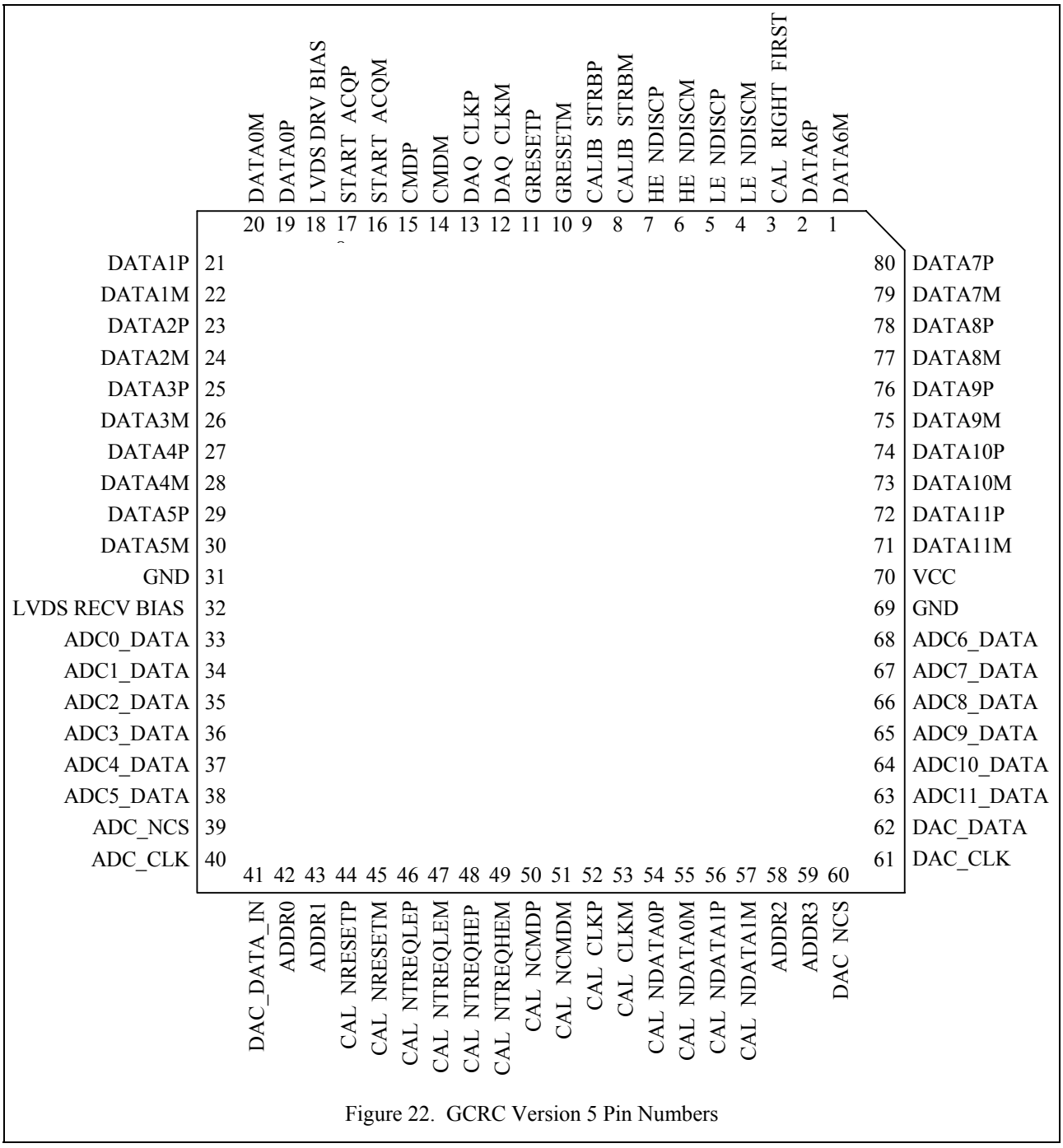

Figure 22. GCRC Version 5 Pin Numbers

Figure 22 shows the pin assigments for the GCRC Version 5 ASIC mounted in a 80 pin QFP package. The package has a body size of 14mm x 14 mm x 2.0 mm thick.